WHAT IS CLAIMED IS:

1. A method of computing cyclical redundancy check bits for a message comprising:

receiving a first word of the message, the first word comprising a plurality of message bits;

computing a plurality of feedforward bits for the first word by logically combining a plurality of the plurality of message bits into a plurality of logical expressions, combining the plurality of logical expressions into a plurality of terms, and storing the plurality of terms as a plurality of feedforward bits;

providing the plurality of feedforward bits to a first logic circuit;

providing a plurality of cyclical redundancy check bits using the first logic circuit;

providing a plurality of feedback bits for the plurality of cyclical redundancy check bits using a feedback circuit; and

providing the plurality of feedback bits to the first logic circuit.

2. The method of claim 1 wherein the first logic circuit is a summing circuit.

3. The method of claim 2 wherein the summing circuit provides an exclusive-or function.

4. The method of claim 2 wherein the feedback circuit is pipelined such that it receives an input and provides a corresponding output two clock cycles later.

5. A method of computing cyclical redundancy check bits for a message comprising:

receiving a first word of the message, the first word comprising a plurality of message bits;

computing a plurality of feedforward bits for the first word using a feedforward circuit, wherein the feedforward circuit receives the first word and provides the plurality of feedforward bits after N clock cycles;

providing the plurality of feedforward bits to a first logic circuit;

providing a plurality of cyclical redundancy check bits using the first logic circuit;

providing a plurality of feedback bits for the plurality of cyclical redundancy check bits using a feedback circuit, wherein the feedback circuit receives the plurality of cyclical redundancy check bits and provides the plurality of feedback bits after 2N clock cycles; and

providing the plurality of feedback bits to the first logic circuit.

6. The method of claim 4 wherein N is equal to one.

7. An integrated circuit comprising:

a circuit configured to receive a message and provide a plurality of cyclical redundancy check bits comprising:

a feedforward circuit; and

a feedback circuit, where an output of the feedforward circuit and an output of the feedback circuit are coupled to a logic circuit, wherein an output of the logic circuit provides the cyclical redundancy check bits, and

wherein the feedforward circuit comprises a first plurality of logic gates coupled to receive the message and provide outputs to a second plurality of logic gates,

wherein at least one of the first plurality of logic gates couple to at least two of the second plurality of logic gates.

8. The integrated circuit of claim 7 wherein the first logic circuit is a summing circuit.

9. The integrated circuit of claim 8 wherein the summing circuit provides an exclusive-or function.

10. The integrated circuit of claim 9 further comprising a plurality of flip-flops coupled to provide outputs to the first plurality of logic gates.

11. The integrated circuit of claim 9 further comprising a plurality of flip-flops coupled to receive inputs from the first plurality of logic gates and provide outputs to the second plurality of logic gates.

12. The integrated circuit of claim 9 further comprising a plurality of flip-flops coupled to receive outputs from the second plurality of logic gates.

13. A receiver for use in data networks comprising an integrated circuit, the integrated circuit comprising:

a first circuit configured to receive words in a data message, wherein each word is a first number of bits in length;

a first summing node configured to receive an output from the first circuit;

a second circuit configured to receive an input from the first summing node and provide an output to the first summing node;

a third circuit coupled to receive an input from the first summing node; and

a second summing node configured to receive an output from the first summing node, an output from the third circuit, and provide a plurality of cyclical redundancy check bits.

14. The receiver of claim 13 wherein the first circuit left shifts each input word by a second number of bits, divides the result by a generator, and provides the remainder as an output.

15. The receiver of claim 14 wherein the second circuit left shifts each input word by twice the first number of bits, divides the result by a generator, and provides the remainder as an output.

16. The receiver of claim 15 wherein the third circuit left shifts each input word by the first number of bits, divides the result by a generator, and provides the remainder as an output.

17. The receiver of claim 16 wherein the first summing node and the second summing node provide an exclusive-OR function.

18. The receiver of claim 16 wherein the first circuit left shifts each input word by a second number of bits, divides the result by a generator, and provides the remainder as an output each third number of clock cycles and the second circuit left shifts each input word by twice the first number of bits, divides the result by a generator, and provides the remainder as an output each fourth number of clock cycles, wherein the fourth number is twice the third number.

19. The receiver of claim 18 wherein the fourth number is two and the third number is one.

20. The receiver of claim 18 wherein the first number is 32.